11-01-04

AF/2134

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No. : 09/429,174 Confirmation No. (None)
Appellants : Jung-Chih Huang, et al.
Filed : October 28, 1999
Title : PRE-BOOT SECURITY CONTROLLER
TC/A.U. : 2134
Examiner : Christopher J. Brown

Docket No. : 2139
Customer No.: 23320

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
Post Office Box 1450
Alexandria, Virginia 22313-1450

Sir:

REQUEST FOR ORAL HEARING

AND

TRANSMITTAL OF
APPEAL REPLY BRIEF

Appellant hereby requests an oral hearing in the above-identified matter. The fee set forth in 37 C.F.R. § 1.17(d) is enclosed.

Enclosed herewith are three (3) copies of an Reply Brief for this patent application together with a check in the amount of the fee set forth in 37 C.F.R. § 1.17(c) for filing a Reply Brief in an appeal.

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If any additional fee is required, the Commissioner for Patents is hereby authorized to charge any deficiency or credit any surplus in any relevant fee to Deposit Account No. 19-0735. A duplicate copy of this transmittal letter is enclosed herewith.

Respectfully submitted,

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Dated: 29 October, 2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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Sir:

REPLY BRIEF

Pursuant to 37 C.F.R. § 1.193, through his undersigned attorney the Appellants submit the following brief, in triplicate, in reply to an Examiner's Answer mailed September 7, 2004.

Argument

Pending claims 1-18 stand rejected under 35 U.S.C. § 103(a) based, essentially, upon a combination of two references. Section (10) of the Examiner's Answer entitled "Grounds of Rejection" declares, on pages 2 and 3, the cornerstone underlying all claim rejections to be:

1. United States Patent no. 4,604,708 entitled "Electronic Security System for Electronically Powered Devices" that issued on August 5, 1986, on a patent application filed by Gainer R. Lewis ("the Lewis patent"); in view of
2. United States Patent no. 5,251,304 entitled "Integrated Circuit Microcontroller With On-Chip Memory and External Bus Interface and Programmable Mechanism for Securing the Contents of On-Chip Memory" which issued on a patent application filed in the names of James M. Sibigtroth, Michael W. Rhoades, George G. Grimmer, Jr. and Susan W. Longwell ("the Sibigtroth, et al. patent").

Because combining the disclosures of the Lewis and Sibigtroth, et al. patents is fundamental to all rejections of claims in the present application, Appellants reiterate in the following abbreviated summaries only two of many reasons, explained in greater detail in the Appeal Brief, why pending claims 1-18 are patentable over that combination of references.

There Exists No Motivation to Combine the Lewis and Sibigtroth, et al. Patents

Page 8 of the Examiner's Answer, **for the first time**[1], provides the following explanation of motivations one of ordinary skill would allegedly have for combining the disclosures of the Lewis and Sibigtroth, et al. patents to obtain the invention claimed in the present application.

> In this case, It would be obvious to one skilled in the art to integrate the controller and memory of Lewis on the specific integrated circuit structure of Sibigtroth **because of its small size, decreased access and increased security**. This knowledge is generally available to one of ordinary skill in the art. Sibigtroth teaches an IC for an electronic device, (Col 2 lines 50-64). (Emphasis supplied.)

The following text appears in column 2 at lines 50-64 of the Sibigtroth, et al. patent.

> There are a variety of applications for a data processor system such as data processing system 10 of FIG. 1. One application is in the area of control applications such as pay-for-view TV control. When data processor 14 is released from a reset condition, it first

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[1] The now abandoned alleged motivation for combining the disclosures of the Lewis and Sibigtroth, et al. patents excerpted from page 4 of the January 14, 2004, Office's Action final rejection of claims appears in its entirety below.

> Sibitroth (sic) discloses a controller and memory as part of an integrated circuit (Sibitroth (sic) Col 2 lines 19-25). It would be obvious to one skilled in the art to construct the microcomputer of Lewis in the method of Sibitroth (sic) because it is more compact.

> addresses memory locations either contained within the integrated circuit portion 11 or within an external memory of peripheral portion 12, depending on how the system is configured. Data processor 14 receives instructions and data for initializing registers (not illustrated) internal to data processor 14. Once the initialization process is complete, data processor 14 executes instructions by addressing memory external to the integrated circuit portion 11 of system 10, for the purpose of controlling peripherals, either internal or external to the integrated circuit portion of data processing system 10, that enables viewing of TV programs in accordance with predetermined guidelines or permissions.

Appellants are unable to find anywhere in the preceding text any disclosure or suggestion of the motivations alleged in the Examiner's Answer of:

1. small size;

2. decreased access; or

3. increased security.

Turning now to those portions of the Lewis and Sibigtroth, et al. patents which expressly disclose those references' respective purposes or motivations, the Lewis patent's stated motivation is theft deterrence.

> **A thief** who removes a device protected by the present invention **will be unable to use the device**, and thus once aware that the device is so protected will likely be deterred from removing it. (Col. 6, lines 59-62) (Emphasis supplied.)

The Sibigtroth, et al. patent identifies the following problems which its invention allegedly solves.

1. There is often a need to prevent read or write accesses to . . . memory elements for various security reasons. (Col. 1, lines 19-21.)

2. [M]emory space within the chip is typically limited, the instructions and data contained within the chip are also limited in size. (Col. 1, lines 32-34.)

3. Another disadvantage with a security feature requiring a single-chip mode of operation is the inability to communicate with any peripheral devices external to the chip. (Col. 1, lines 38-41.)

Because neither the Lewis patent nor the Sibigtroth, et al. patents disclose nor do they suggest that there exists any size, decreased access or increased security problems, Appellants respectfully submit that the motivation alleged **for the first time** in the Examiner's Answer for combining the references comes not from the cited references, nor does it come from any general desire to provide enhanced theft deterrence for electronic devices. Rather, Appellants respectfully submit that the motivation to combine the Lewis and Sibigtroth, et al. patents expressed **for the first time** in the Examiner's Answer comes from a need cobble the two references together to provide a basis for rejecting claims pending in the present patent application.

Objective Evidence of Patentability:
Failure of Others

Condensed to its essentials, the Appeal Brief's exposition of objective evidence of patentability proves:

1. the Lewis patent's expressly declared purpose, as excerpted both above and below, is theft deterrence;

2. the combined disclosures of the Lewis and Sibigtroth, et al. patents provide no theft deterrence; and

3. the invention encompassed by pending claims 1-18 provides effective theft deterrence.

Beginning in column 6 at line 59 the Lewis patent expressly declares its purpose, i.e. declares a property which the invention disclosed in that reference must possesses, as being:

> **[a] thief** who removes a device protected by the present invention **will be unable to use the device**, and thus once aware that the device is so protected will likely be deterred from removing it. (Emphasis supplied.)

Avoiding the preceding issue, one searches the Examiner's Answer in vain for any citation to column 6 in the Lewis patent, the text excerpted above, the word "thief" or any similar word like "theft" etc. That is, **the Examiner's Answer avoids mentioning the stated purpose both for the primary reference, and for the present invention**.

Immediately below the section heading "(11) Response to Argument," the Examiner's Answer in only one place on page 6 obliquely alludes to the Appeal Brief's detailed proofs that the Lewis patent fails to provide that reference's necessary property.

> The Examiner has reviewed the declaration of the inventor Brian Oh. The declaration, on paper 14, relates to the degree of security, not whether or not security exists.

> The relative amount of security is not reflected in the claim limitations.

As implied by the Examiner's Answer failure to mention any other theft deterrence text in the Appeal Brief, **does only one obscure paragraph in Appendix II to the Appeal Brief truly present the only argument in that Brief's seventy-five (75) pages which addresses the combined Lewis and Sibigtroth, et al. patents' failure to provide theft deterrence**?

Similar to the failure of the Examiner's Answer to even mention the text excerpted above from column 6 in the Lewis patent or that reference's stated purpose, one also searches the Examiner's Answer in vain for any mention of arguments, which appear on pages 41-48 of the Appeal Brief, proving that the combined Lewis and Sibigtroth patents fail to provide any theft deterrence. Disregarded pages 41-48 in the Appeal Brief explain in detail:

1. how the combined disclosures of the Lewis and Sibigtroth, et al. patents fail to provide any theft deterrence; and
2. why, for that reason, controlling legal authority, summarized on pages 39 through 41 of the Appeal Brief, mandates that the references' failure to provide theft deterrence objectively proves that claims 1-18 are patentable.

It serves no useful purpose to repeat here the detailed explanation, appearing on pages 41-48 of the Appeal Brief, which conclusively proves that the combined disclosures of the Lewis and Sibigtroth, et al. patents fail to provide theft deterrence. However, the detailed explanation appearing on pages 41-48, particularly pages 46 and 47 therein, proves that if the microcomputer 10 of the Lewis patent were constructed in the method of the Sibigtroth, et al. patent as stated in the final rejection of this application's claims, passwords stored there are easily, quickly and non-destructively retrievable using a widely available device called an in-circuit emulator ("ICE").

Since passwords stored in the microcomputer 10 of the Lewis patent when constructed in the method of the Sibigtroth are easily, quickly and non-destructively retrievable using an ICE, how can the Examiner's Answer possibly implicitly maintain that those combined references provide any theft deterrence? Conversely, the invention encompassed by claims 1-18 locates both stored passwords and a password-comparing digital logic circuit within a single integrated circuit which inherently prevents accessing the stored password by any technique other than, perhaps, discarding or destroying the password storing integrated circuit. Thus, the invention encompassed by pending claims 1-18 truly provides the theft deterrence sought by the Lewis patent, and that the combined Lewis and Sibigtroth, et al. patents do not provide.

Applying the holdings of In re Gurley[2], In re Sponnoble[3] and In re Caldwell[4], the failure of the combined disclosures of the Lewis and Sibigtroth, et al. patent to provide theft deterrence **actually discourages a person of ordinary skill from following the path set out in that reference**. Moreover, a combination of those references "teaches away if it leaves the impression that the product would not have the property sought by the applicant." In re Gurley supra citing In re Caldwell. Paraphrasing the Supreme Court's decision in Adams[5], that in 1986 Lewis may have been able to convince a United States patent examiner to issue a patent on his device has little significance in the light of the foregoing.

Conclusion

As explained in the preceding summary and in the Appeal Brief, there truly exists no motivation to combine the Lewis and Sibigtroth, et al. patents other than this application's pending claims.

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[2] 7 F.3d 551, 31 USPQ2d 1130 (Fed. Cir. 1994)

[3] 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969)

[4] 319 F.2d 254, 256, 138 USPQ 243, 245 (CCPA 1963)

[5] 383 U.S. 39, 50, 148 USPQ 479, 483 (1966)

Furthermore, as also explained in the preceding summary and in the Appeal Brief, controlling authority cited above declares that the failure of the combined references to produce theft deterrence:

1. mandates that the pending claims are patentably non-obvious;
2. actually discourages a person of ordinary skill from following the path set out in the combined references; and
3. teaches away from the claimed invention because the combined references leave the impression to one of ordinary skill in the art that their combination lacks the desired property of theft deterrence.

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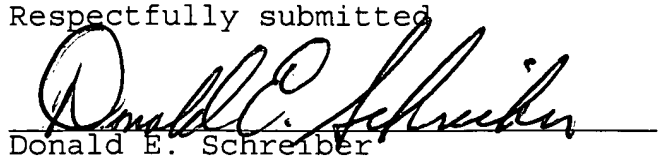
For the reasons set forth above and in the Appeal Brief, Appellants respectfully request that the rejection of claims in the January 14, 2004, Office Action be reversed, and claims 1-18 now pending in this patent application be declared patentable.

Respectfully submitted



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